Amendments to the Claims:

This listing of claims replaces all prior versions, and listings, of claims in this application.

Listing of Claims:

1. (Currently Amended) A frequency synthesizer, comprising:

a divider for receiving a reference clock with a substantially fixed period and generating an output clock with a time-varying period;

a noise-shaped quantizer for quantizing a period control word to a time-varying value in response to said output clock fed from said divider so that said divider generates said output clock by means of dividing said reference clock by said time-varying value; and

a filter for substantially filtering out jitter from said output clock,

wherein said period control word has a bit resolution greater than that of said time-varying value.

2. (Canceled)

3. (Original) The frequency synthesizer as claimed in claim 1, wherein said noise-shaped quantizer is a delta-sigma quantizer.

4. (Original) The frequency synthesizer as claimed in claim 1, wherein said filter is an analog phase locked loop (PLL) device as a low pass filter for removing high frequency jitter from said output clock.

5. (Currently Amended) A frequency synthesizer, comprising:

a noise-shaped quantizer for quantizing a period control word to a time-varying value; and

a divider for generating an output signal by means of dividing a reference signal by said time-varying value, said output signal feeding back to said noise-shaped quantizer so that said noise-shaped quantizer generates said time-varying value in response to said feedback output signal,

wherein said period control word has a bit resolution greater than that of said time-varying value.

6. (Original) The frequency synthesizer as claimed in claim 5, further comprising a filter for of significantly filtering out jitter from said output signal.

7. (Original) The frequency synthesizer as claimed in claim 6, wherein said filter is an analog phase locked loop (PLL) device as a low pass filter for removing high frequency jitter from said output signal.

8. (Original) The frequency synthesizer as claimed in claim 5, wherein said reference signal is a reference clock with a substantially fixed period.

9. (Original) The frequency synthesizer as claimed in claim 5, wherein said output signal is an output clock with a time-varying period and a substantially precise long-term average frequency.

10. (Canceled)

11. (Original) The frequency synthesizer as claimed in claim 5, wherein said noise-shaped quantizer is a delta-sigma quantizer.

12. (Currently Amended) A frequency synthesizer, comprising:

means for quantizing a period control word to a time-varying value; and

means for generating an output signal by means of dividing a reference signal by said time-varying value, said output signal feeding back to said means for quantizing said period control word so that said time-varying value is generated in response to said feedback output signal,

wherein said period control word has a bit resolution greater than that of said time-varying value.

13. (Original) The frequency synthesizer as claimed in claim 12, further comprising means for of significantly filtering out jitter from said output signal.

14. (Original) The frequency synthesizer as claimed in claim 13, wherein said means for filtering the jitter is an analog phase locked loop (PLL) device as a low pass filter for removing high frequency jitter from said output signal.

15. (Original) The frequency synthesizer as claimed in claim 12, wherein said reference signal is a reference clock with a substantially fixed period.

16. (Original) The frequency synthesizer as claimed in claim 12, wherein said output signal is an output clock with a time-varying period and a substantially precise long-term average frequency.

17. (Canceled)

18. (Original) The frequency synthesizer as claimed in claim 12, wherein said means for quantizing said period control word is a delta-sigma quantizer.